Application Note 162: Oct 02, 1995

Memory-Backup Supply is Simple And Efficient

A simple design of a memory backup supply is done with the MAX921 comparator and reference circuit in conjunction with a JFET and some discrete components. This circuit provides an output of 5V at 1mA with an input range of 8V to 32V.

The high-efficiency RAM-backup power supply of **Figure 1** delivers 5V at 1mA for inputs in the range 8V to 32V. Most single-chip regulators that operate over this range are bipolar ICs with quiescent currents comparable to the 1mA load current. This circuit, however, draws only 10µA when operating.

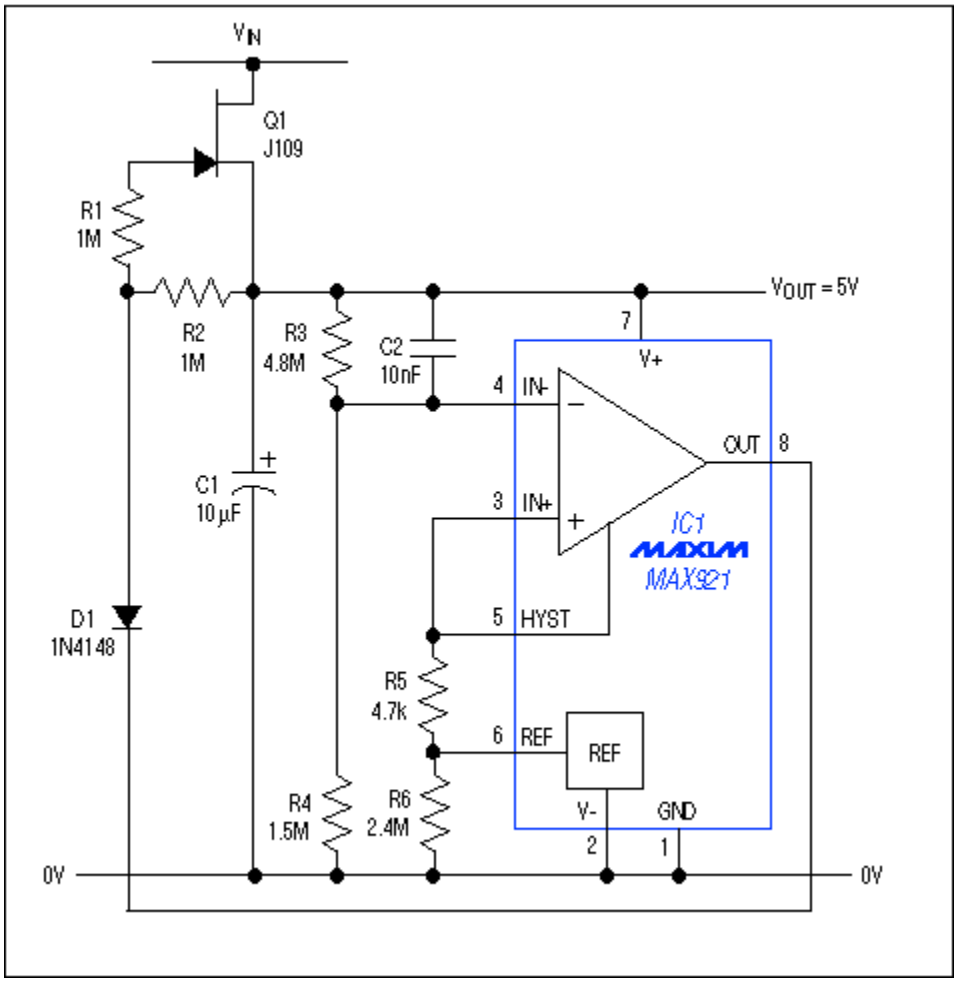

Figure 1. This simple RAM-backup power supply offers efficiency and versatility.

The JFET series-pass element operates as a switched current source in a switched linear regulator: at start-up, C1 is fully discharged and Q1 acts as a current source. VOUT rises linearly as C1 charges, activating IC1 at 2V and continuing toward the 5V threshold set by R3 and R4. IC1 combines a CMOS micropower comparator and 1.182V bandgap reference. As VOUT reaches its threshold, the comparator output goes low, turning off Q1 by reverse-biasing its gate-source junction. As the load current discharges C1 below the output threshold, Q1 turns back on and completes one switching cycle.

Q1's depletion characteristic ensures start-up for the circuit. It also ensures excellent PSRR (>60dB for 5.5V $\leq$ VIN $\leq$ 30V), because both the reference and the error amplifier receive power from the regulated output voltage. Q1 should be chosen for IDSS, VGS(OFF), and VDS. IDSS is the current drawn at start-up, when Q1 is saturated (i.e., when VGS is zero and VDS $\geq$ VGS(OFF)). VGS(OFF), which determines the minimum allowed VIN-VOUT difference for proper circuit operation, must be less than VOUT to ensure that Q1 can turn off. The Q1 device shown in the prototype circuit (J109) specifies a minimum IDSS of 40mA, a VGS(OFF) between -6V and -2V, and a minimum VDS of 25V. For production, a J113 type is more appropriate.

C2 reduces output ripple by speeding the propagation of feedback to the comparator's inverting input. Without C2, the high value of R3 (necessary to minimize the circuit's quiescent current) combines with parasitic capacitance to slow the regulator's response. The value shown (10nF) lowers the sawtooth-ripple voltage from 200mVp-p to 20mVp-p. Larger C1 values further decrease the ripple while increasing the circuit's off time, which also reduces the average supply current. R1 and R2 determine the on time. R1 also limits the turn-off spikes produced by rapid high-to-low transitions on the gate of Q1.

IC1's pin 5 (HYST) lets the user add comparator hysteresis, adjustable via R5 and R6. The R6 value shown (2.4MW) makes the hysteresis value in mV (about 5mV in this case) numerically equal to the R5 value in kW.

A related idea appeared in the 10/2/95 issue of Electronic Design.

MORE INFORMATION

MAX921: QuickView -- Full (PDF) Data Sheet (152k) -- Free Sample